WHAT IS CLAIM IS:

1. An a-WO_3 gate ISFET device, comprising:

a semiconductor substrate;

a gate oxide layer on the semiconductor substrate;

an a-WO_3 layer overlying the gate oxide layer to form an a-WO_3 gate;

a source/drain in the semiconductor substrate beside the a-WO_3 gate;

a metal wire on the source/drain; and

a sealing layer overlying the metal wire, and exposing the a-WO_3 layer.

2. The device as claimed in claim 1, wherein the length of the channel, the width of the channel and ratio of width/length of the channel of the ISFET is about 50μm, 1000μm, and 20 respectively.

3. The device as claimed in claim 1, wherein the semiconductor substrate is P-type.

4. The device as claimed in claim 1, wherein the resistivity of the semiconductor substrate ranges from 8 to 12 Ω·cm.

5. The device as claimed in claim 1, wherein the lattice parameter of the semiconductor is (1,0,0).

6. The device as claimed in claim 1, wherein the thickness of the gate oxide is about 1000Å.

7. The device as claimed in claim 1, wherein the thickness of the tungsten oxide layer is at least 1000Å.

8. The device as claimed in claim 1, wherein the metal wire consists of Al.

9. The device as claimed in claim 1, wherein the sealing layer consists of epoxide resin.

10. The device as claimed in claim 1, wherein the source/drain is N-type.

11. The device as claimed in claim 10, wherein the N-type impurities within the source/drain consist of phosphorous.

12. A method for fabricating an a-WO_3 gate ISFET device, comprising the following steps:

providing a semiconductor substrate;

forming an imaginary gate on the semiconductor substrate to define the gate area of the ISFET;

forming a source/drain in the semiconductor substrate beside the imaginary gate;

removing the imaginary gate; and

forming an a-WO_3 gate in the gate area to form a ISFET.

13. The method as claimed in claim 12, wherein the semiconductor substrate is P-type.

14. The method as claimed in claim 12, wherein the

resistivity of the semiconductor substrate ranges from 8 to 12 Ω·cm.

15. The method as claimed in claim 12, wherein the lattice parameter of the semiconductor is (1,0,0).

16. The method as claimed in claim 12, wherein the imaginary gate consists of silicon dioxide.

17. The method as claimed in claim 12, wherein the thickness of the imaginary gate is about 5000Å.

18. The method as claimed in claim 12, wherein the imaginary gate is removed by means of wet-etching.

19. The method as claimed in claim 12, wherein the step of forming an imaginary gate in the semiconductor gate to define a gate area of the ISFET comprises:

cleaning the semiconductor substrate;

forming a pad oxide layer on the semiconductor substrate; and

removing a portion of the pad oxide layer to form an imaginary gate to define the area of the gate.

20. The method as claimed in claim 19, wherein the pad oxide layer is formed by means of wet oxidation.

21. The method as claimed in claim 19, wherein the step of removing a portion of the pad oxide layer is completed by means of wet etching.

22. The method as claimed in claim 12, wherein the step of forming a source/drain beside the imaginary gate comprises:

doping the semiconductor substrate by using the imaginary gate as a mask to form a source/drain.

23. The method as claimed in claim 22, wherein the dose of the dopants is about 10^{15}atoms/cm^2.

24. The method as claimed in claim 12, wherein the step of forming an a-WO_3 gate in the gate area comprises:

forming a gate oxide layer on the gate area; and

forming an a-WO_3 layer on the gate oxide to form a a-WO_3 gate.

25. The method as claimed in claim 24, wherein the thickness of the gate oxide layer is about 1000Å.

26. The method as claimed in claim 24, wherein the gate oxide consists of silicon dioxide.

27. The method as claimed in claim 24, wherein the a-WO_3 gate is formed by RF-sputtering.

28. A method for fabricating an a-WO_3 gated ISFET, comprising following steps:

providing a P-type semiconductor substrate;

forming a pad oxide layer on the semiconductor layer;

removing a portion of the pad oxide layer to form an imaginary gate to define a gate area;

doping the semiconductor substrate by using the imaginary gate as a mask to form a source/drain beside the imaginary gate;

removing the imaginary gate;

forming a gate oxide layer on the semiconductor substrate; and

forming an a-WO_3 layer on the gate oxide layer to form an a-WO_3 gate.

29. The method as claimed in claim 28, wherein the resistivity of the semiconductor substrate ranges from 8 to 12 $\Omega \cdot cm$.

30. The method as claimed in claim 28, wherein the lattice parameter of the semiconductor is (1,0,0).

31. The method as claimed in claim 28, wherein the thickness of the imaginary gate is about 5000Å.

32. The method as claimed in claim 12, wherein the pad oxide layer is formed by means of wet oxidation.

33. The method as claimed in claim 28, wherein the step of partially removing the pad oxide layer is performed by wet etching.

34. The method as claimed in claim 28, wherein the dopants used for doping consist of phosphorous.

35. The method as claimed in claim 28, wherein the

dose of the dopants is 10^{15}atoms/cm^2.

36. The method as claimed in claim 28, wherein the imaginary gate is removed by wet etching.

37. The method as claimed in claim 28, wherein the gate oxide layer consists of silicon dioxide.

38. The method as claimed in claim 28, wherein the thickness of the gate oxide layer is about 1000Å.

39. The method as claimed in claim 28, wherein the a-WO_3 layer is formed by RF-sputtering.